CECS 225

Lab1

Thanh Le

**Section 1**: HalfAdder Verilog module source

`timescale 1ns / 1ps

module HalfAdder(A, B, Cout, S);

input A, B;

output Cout, S;

assign Cout = A & B;

assign S = A ^ B;

endmodule

**Section 2**: HalfAdder Verilog Test Fixture

`timescale 1ns / 1ps

module HalfAdder\_Tester;

// Inputs

reg A;

reg B;

// Outputs

wire Cout;

wire S;

// Instantiate the Unit Under Test (UUT)

HalfAdder uut (

.A(A),

.B(B),

.Cout(Cout),

.S(S)

);

initial begin

// test case 0

A = 0;

B = 0;

#10; //wait 10 time units

A = 0;

B = 1;

#10; //wait 10 time units

A = 1;

B = 0;

#10; //wait 10 time units

A = 1;

B = 1;

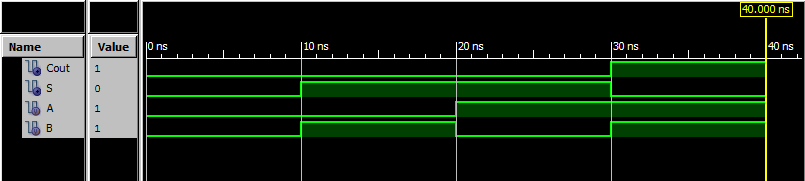
#10; //wait 10 time units

$stop; //end the stimulation

end

endmodule

**Section 3**: HalfAdder Simulation Screenshot



**Section 4**: FullAdder Verilog module source

`timescale 1ns / 1ps

module FullAdder(FA\_A, FA\_B, Cin, FA\_S, Cout);

input FA\_A, FA\_B, Cin;

output FA\_S, Cout;

wire ha0\_S, ha0\_C, ha1\_C;

HalfAdder ha0( .A( FA\_A ),

.B( FA\_B ),

.Cout( ha0\_C ),

.S( ha0\_S )

);

HalfAdder ha1( .A( Cin ),

.B( ha0\_S ),

.Cout( ha1\_C ),

.S( FA\_S )

);

assign Cout = ha0\_C | ha1\_C;

endmodule

**Section 5**: FullAdder Verilog Test Fixture

`timescale 1ns / 1ps

module FullAdder\_Tester;

// Inputs

reg FA\_A;

reg FA\_B;

reg Cin;

// Outputs

wire FA\_S;

wire Cout;

// Instantiate the Unit Under Test (UUT)

FullAdder uut (

.FA\_A(FA\_A),

.FA\_B(FA\_B),

.Cin(Cin),

.FA\_S(FA\_S),

.Cout(Cout)

);

initial begin

// test case 0

FA\_A = 0;

FA\_B = 0;

Cin = 0;

#10; //wait 10 time units

// test case 1

FA\_A = 0;

FA\_B = 1;

Cin = 0;

#10; //wait 10 time units

// test case 2

FA\_A = 1;

FA\_B = 0;

Cin = 0;

#10; //wait 10 time units

// test case 3

FA\_A = 1;

FA\_B = 1;

Cin = 0;

#10; //wait 10 time units

// test case 4

FA\_A = 0;

FA\_B = 0;

Cin = 1;

#10; //wait 10 time units

// test case 5

FA\_A = 0;

FA\_B = 1;

Cin = 1;

#10; //wait 10 time units

// test case 6

FA\_A = 1;

FA\_B = 0;

Cin = 1;

#10; //wait 10 time units

// test case 7

FA\_A = 1;

FA\_B = 1;

Cin = 1;

#10; //wait 10 time units

$stop; //end the stimulation

end

endmodule

**Section 6**: FullAdder Simulation Screenshot

